PATENT APPLICATION
DOCKET NO.: 10010788-1

REMARKS

Claims 1-20 were originally presented for examination, of which claims 1, 11 and 15 are currently amended. New claims 21-29 are added by way of the present response. Of the currently pending claims 1-29, claims 1, 11 and 21 are in independent form.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Objections to the Specification

The section having the heading "CROSS-REFERENCE TO RELATED APPLICATION(S)" on Page 1 of the original specification has been amended by way of a replacement section to address the minor informalities identified in the outstanding Office Action.

Also, the specification is objected to in the Office Action because of the usage of "SYNC" therein. The Examiner has commented that "trademarks are usually denoted by capitalizing all letters of their names, therefore, "SYNC" should be changed to "sync" to avoid any potential confusion as to whether this terminology is a trademark. Appropriate correction is required."

Applicant respectfully traverses this objection and submits that the Manual of Patent Examining Procedure (MPEP) merely provides that if a trademark is used in a patent application, it should be capitalized wherever it appears and be accompanied by the generic terminology. MPEP §608.01(v). There is no

prohibition as such, however, against using capital letters for terms in a specification. Further, Applicant contends that the term "SYNC" is well known in the art, and it is commonly used with all capital letters by those skilled in the art. By way of example, Applicant points out that in U.S. Patent No. 6,707,626 to Esumi and U.S. Patent No. 6,744,697 to Mitra et al., two recently issued U.S. patents, the term "SYNC" is used with all capital letters to describe appropriate signals. Applicant therefore submits that there is no basis for confusion as to whether Applicant's use of this terminology is in the nature of a trademark. Accordingly, Applicant respectfully requests that this objection be withdrawn.

Regarding the Claim Rejections - 35 U.S.C. §102(e)

Claims 1 and 11-14 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,516,362 to Magro et al. (hereinafter the *Magro* reference). The following comments were provided in connection with the base claims 1 and 11:

> As per claim 1, Magro taught an invention for synchronizing a first circuit portion [FIG. 2B, item 104] operating in a first clock domain that is clocked with a first clock signal [GIG. 2B, item 106] and a second circuit portion [FIG. 2B, item 130] operating in a second clock domain that is clocked with a second clock signal [FIG. 2B, item 110], the invention comprising of:
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> - Means for generating a sync pulse signal [FIG. 3A, item 206] based on a predetermined temporal relationship between a first and

second clock signals [column 8, lines 22-27, lines 30-33]; and

- A clock synchronizer controller operable to generate a plurality of control signals based on sync pulse signal [column 6, lines 64-66], said clock synchronizer controller including a sync adjuster operable to re-position said sync pulse signal based on a skew between said first and second clock signals [column 9, lines 53-67; column 10, lines 34-49], wherein a least a portion of said plurality of control signals actuate data transfer synchronizer circuitry disposed between said first and second circuit portions [column 7, lines 59-66; column 12, lines 33-50].

As per claim 11, Magro taught an invention for synchronizing data transfer operations between two circuit portions across a clock domain boundary [abstract]:

- Generating a secondary clock signal from a primary clock signal [FIG. 2B, item 108], wherein said primary clock signal [FIG. 2B, item 106] is operable to clock a first circuit portion [FIG. 2B, item 104] and said secondary clock signal [FIG. 2B, item 110] is operable to clock a second circuit portion [FIG. 2B, item 20];
- Generating a sync pulse signal [FIG. 3A, item 206] based on a predetermined temporal relationship between said primary and secondary clock signals [column 8, lines 22-27, lines 30-33];
- Compensating for a skew between said primary and secondary clock signals and adjusting said sync pulse signal, if necessary [column 10, lines 34-49]; and
- Generating data transfer control signals at appropriate times relative to said primary and secondary clock signals [column 7, lines 59-66; column 12, lines 33-50] based on said sync pulse signal [column 9, lines 53-67] to control data transfer operations between said first and second circuit portions.

Applicant respectfully submits that the foregoing §102(e) claim rejections have been overcome or otherwise rendered moot by the present response. The present invention, as defined by the base claim 1, is directed to a system for synchronizing a first circuit portion operating in a first clock domain (clocked with a first clock signal) and a second circuit portion operating in a second clock domain (clocked with a second clock signal). A SYNC pulse signal is generated based on occurrence of a coincident edge between the first and second clock signals. A clock synchronizer controller is provided for generating a plurality of control signals based on the SYNC pulse signal, which clock synchronizer controller includes a SYNC adjuster operable to re-position the SYNC pulse signal based on a new coincident edge between the first and second clock signals that is defined in response to a skew between the clock signals.

In a further aspect, the currently-amended claim 11 is drawn to a method of synchronizing data transfer operations between two circuit portions across a clock domain boundary. As presently constituted, claim 11 includes, *inter alia*, generating a SYNC pulse signal based on occurrence of a coincident edge between primary and secondary clock signals, and adjusting the SYNC pulse signal to re-position it based on a new coincident edge that is defined response to a skew between the clock signals.

In contrast, the *Magro* reference does not teach or suggest generating a SYNC pulse signal based on occurrence of a coincident edge between two clock signals. Also, it does not teach or suggest a SYNC adjuster operable to re-position the SYNC pulse signal based on a new coincident edge between the two clock signals that is defined in response to a skew between the clock signals. More specifically, the *Magro* reference teaches a synchronization signal called phase_sync signal 206 that is generated when the rising edge of a delayed slow clock signal, i.e., clk_cpu clock signal 106, always lags behind the corresponding rising edge of the faster clock signal, i.e., clk_mem clock signal 110. See FIG. 3a and FIG. 3b; see also col. 8, lines 6-38. Further, because the phase_sync signal 206 is generated within the faster clock domain, i.e, in the clk_mem frequency domain, the phase_sync signal 206 exhibits the same skew as the clk_mem clock signal 110. There is absolutely no teaching or even a scintilla of suggestion with respect to adjusting the phase_sync signal 206 in order to re-position it based on a new coincident edge between the clk_mem and clk_cpu signals.

Based on the foregoing, Applicant respectfully submits that the base claims 1 and 11 are allowable over the *Magro* reference. Further, the dependent claims 2-10 and 12-20 respectively depend from and further limit the base claims 1 and 11, and are

therefore also deemed to be allowable over the *Magro* reference for the reasons set forth above.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

In the outstanding Office Action, claim 18 is rejected under 35 U.S.C. §103(a) as being unpatentable over the *Magro* reference (as applied to the base claim 11) in view of U.S. Patent No. 5,987,081 to Csoppenszky et al. (hereinafter the *Csoppenszky* reference). Further, claims 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Magro* reference (as applied to the base claim 11). The following comments were provided in connection with these §103(a) rejections:

> Magro taught a synchronizer for transferring data between two different clock domains by generating various data transfer control signals [column 6, lines 64-66] for the data transfer synchronizer circuitry [FIG. 2B, item 130] disposed between the first and second circuit portions.
> However, Magro did not disclose expressly the details of configuration in which the data transfer control signals are transferred.
>
> Csoppenszky taught a synchronizer for data transfer between clock domains [abstract], the synchronizer comprising of data transfer control signals that are staged through a plurality of registers [column 6, lines 7-36].
>
> An ordinary artisan at the same time the invention was made would have been motivated to look for a stable way to transfer data in a system with two different clock domains [see Csoppenszky: column 1, lines 11-45].
>
> Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Magro and

Csoppenszky because of the aforementioned motivation and also their involvement in similar problems regarding the synchronization of data transfer in a two-clock domain system.

Magro taught a synchronizer for transferring data between two different clock domains. However, Magro did not disclose expressly the source for the two different clocks.

It would have been obvious to an ordinary artisan to utilize a core clock for the primary clock signal and a bus clock for the secondary clock signal because Applicant has not disclosed an advantage, a particular purpose, or solution to a stated problem for each of the respective clock source. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with other clock sources because the Applicant's invention is intended to synchronize two different clock signals, irrelevant of their generating sources.

Therefore, it would have been obvious to one of ordinary skill in the art to use a core clock for the primary clock signal and a bus clock for the secondary clock signal to obtain the invention as specified in claims 19 and 20.

Applicant respectfully submits the pending §103(a) rejections have been overcome or otherwise rendered moot by the present response. As discussed above with respect to the base claim 11, the *Magro* reference does not suggest or even remotely allude to the claimed limitations of generating a SYNC pulse signal based on occurrence of a coincident edge between two clock signals and adjusting the SYNC pulse signal to re-position it based on a new coincident edge that is defined responsive to a skew between the two clock signals. Applicant further submits that reliance on the *Csoppenszky* reference is of no avail in this regard. The *Csoppenszky* reference is directed to a method and

apparatus for deterministically transferring data across an asynchronous boundary in a test environment. Col. 2, lines 40-42. A synchronizer comprising a series of flip-flops is provided for effectuating data transfer from one clock domain to a second clock domain operating at a higher clock frequency. Col. 2, lines 43-46. A clock enable signal is defined so as to approximately align the enabled rising edges of the faster clock signal with the falling edges of the slower clock signal. This approximate alignment provides a timing window of one half period of the slower clock for the data to stabilize at the input of a flip-flop in the faster clock domain before it is sampled. Col. 2, lines 54-57.

It is well known that to establish obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the combined references must teach or suggest all the claim limitations. MPEP §2143. Applicant respectfully contends that there is no suggestion or motivation in either of the applied references to combine the teachings therein so as to achieve the claimed invention wherein a SYNC pulse signal is generated based on occurrence of a coincident edge between two clock signals, which SYNC pulse signal is operable to be adjusted so as to re-position it based on a new coincident edge that is

defined responsive to a skew between the two clock signals. In addition, the combination of the *Magro* and *Csoppenszky* references fails to teach or suggest all of the limitations of the present invention as currently claimed. Accordingly, Applicant respectfully submits that each of claims 18-20, which are dependent from the base claim 11, is patentable over the applied combination of the references.

Regarding the New Claims 21-29

Applicant has added new claims 21-29 covering the subject matter to which Applicant believes it is entitled. No new matter is introduced. The new base claim 21 recites language that covers the subject matter identified in the pending Office Action to be allowable. Accordingly, the new base claim 21 and the dependent claims 22-29 depending therefrom are believed to be in condition for allowance.

Regarding the Allowable Subject Matter

Applicant gratefully appreciates the indication in the pending Office Action that claims 2-10 and 15-17 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In view of the present amendment, it is believed that claims 2-10 and 15-17 are in condition for allowance.

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Regarding the Art Cited but not Relied Upon

Applicant appreciates the inclusion of the art cited but not relied upon in the pending Office Action. Upon review thereof, it is believed that the currently claimed invention is patentable over the entire art made of record.

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SUMMARY AND CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejections and allow claims 1-29 presented for reconsideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested.

Respectfully submitted,

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